

What is claimed is:

1. A thin film transistor substrate, comprising:
 - a substrate;
 - a gate electrode on said substrate;
 - a gate insulation layer on said gate electrode and on said substrate;
 - an active layer on said gate insulation layer;
 - a source electrode on said active layer and over said gate electrode;
 - a drain electrode on said active layer and that is spaced apart from said source electrode, said drain electrode having a first side facing said source electrode and a second side;
 - a protection layer on said source electrode, on a portion of said drain electrode, on said active layer, and on said gate insulation layer, wherein said first side of said drain electrode is covered by said protection layer, and wherein said second side is not covered by said protection layer; and
 - a pixel electrode in electrical contact with the second side of said drain electrode.
2. A thin film transistor substrate according to claim 1, wherein said pixel electrode overlaps an edge of said second side of said drain electrode.
3. A thin film transistor substrate according to claim 1, said drain electrode has a bent shape.
4. A thin film transistor substrate according to claim 1, wherein said pixel electrode contacts said gate insulation layer.
5. A thin film transistor substrate according to claim 1, further comprising:

a gate line having a gate pad, wherein said gate line electrically connects to said gate electrode;
a gate pad hole through said gate insulation layer and through said protection layer such that said gate pad is at least partially exposed; and
a gate pad electrode electrically contacting said gate pad via said gate pad contact hole.

6. A thin film transistor substrate according to claim 5, wherein a peripheral portion of said gate pad has a bent shape.

7. A thin film transistor substrate according to claim 5, wherein said gate pad electrode contacts said substrate.

8. A thin film transistor substrate according to claim 1, further comprising:
a data line having a data pad, wherein said data line electrically connects to said source electrode;
a data pad hole through said protection layer such that said data pad is at least partially exposed; and
a data pad electrode electrically contacting said data pad via said data pad contact hole.

9. A thin film transistor substrate according to claim 8, wherein said data pad has a bent shape.

10. A thin film transistor substrate according to claim 8, wherein said data pad electrode contacts said gate insulation layer.

11. A method of fabricating a thin film transistor substrate, comprising:
forming a gate electrode on a substrate;

forming a gate insulation layer on the gate electrode and on the substrate;
forming an active layer on the gate insulation layer;
forming source and drain electrodes on the active layer to form a thin film transistor, the source and drain electrodes being spaced apart from each other and located over the gate electrode, wherein the drain electrode has a first side facing the source electrode and a second side;
forming a protection layer on the thin film transistor and on the gate insulation layer, wherein the protection layer covers the first side but not the second side of the drain electrode; and
forming a pixel electrode in electrical contact with the second side of the drain electrode, wherein the pixel electrode is formed using a back exposure.

12. A method of fabricating a thin film transistor substrate according to claim 11, wherein the pixel electrode is formed overlapping the second side.

13. A method of fabricating a thin film transistor substrate according to claim 11, wherein the pixel electrode is formed of a transparent conductive material.

14. A method of fabricating a thin film transistor substrate according to claim 13, wherein the transparent conductive material is selected from a group consisting of indium-tin-oxide (ITO) and indium-zinc-oxide (IZO).

15. A method of fabricating a thin film transistor substrate according to claim 11, wherein the pixel electrode is formed in contact with the gate insulation layer.

16. A method of fabricating a thin film transistor substrate according to claim 11, further including:

forming a gate line on the substrate, wherein the gate line includes a gate pad, and wherein the gate line is formed in electrical contact with the gate

electrode;

covering the gate pad with the gate insulation layer and the protection layer;

forming a contact hole through the gate insulation layer and through the protection layer to expose at least part of the gate pad; and

forming a gate pad electrode that electrically contacts the gate pad through the contact hole.

17. A method of fabricating a thin film transistor substrate according to claim 16, wherein the gate pad is formed with a bent shape.

18. A method of fabricating a thin film transistor substrate according to claim 16, wherein the gate pad electrode is formed on the substrate.

19. A method of fabricating a thin film transistor substrate according to claim 11, further including:

forming a data line on the gate insulation layer, wherein the data line includes a data pad, and wherein the data line is formed in electrical contact with the source electrode;

covering the data pad with the protection layer;

forming a contact hole through the protection layer to expose at least part of the data pad; and

forming a data pad electrode that electrically contacts the data pad through the contact hole.

20. A method of fabricating a thin film transistor substrate according to claim 19, wherein the data pad is formed with a bent shape.

21. A method of fabricating a thin film transistor substrate according to claim

19, wherein the data pad electrode is formed on the gate insulation layer.

22. A liquid crystal display, comprising:

a substrate;

a gate electrode on said substrate;

a gate insulation layer on said gate electrode and on said substrate;

an active layer on said gate insulation layer and over said gate electrode;

a source electrode on said active layer and over said gate electrode;

a drain electrode on said active layer and spaced apart from said source electrode, said drain electrode having a first side facing said source electrode and a second side;

a protection layer on said source electrode, on a portion of said drain electrode, on said active layer, and on said gate insulation layer, wherein said first side of said drain electrode is covered by said protection layer, and wherein said second side is not covered by said protection layer; and

a pixel electrode in electrical contact with said second side of said drain electrode.

23. A liquid crystal display according to claim 22, wherein said pixel electrode overlaps an edge of said second side of said drain electrode.

24. A liquid crystal display according to claim 22, wherein said drain electrode has a bent shape.

25. A liquid crystal display according to claim 22, wherein said pixel electrode contacts said gate insulation layer.

26. A liquid crystal display according to claim 22, further comprising:
a gate line having a gate pad, wherein said gate line electrically connects

to said gate electrode;

a contact hole through said gate insulation layer and through said protection layer such that said gate pad is at least partially exposed; and

a gate pad electrode electrically contacting said gate pad via said contact hole.

27. A liquid crystal display according to claim 26, wherein a peripheral portion of said gate pad has a bent shape.

28. A liquid crystal display according to claim 26, wherein said gate pad electrode contacts said substrate.

29. A liquid crystal display according to claim 22, further comprising:
a data line having a data pad, wherein said data line electrically connects to said source electrode;

a contact hole through said protection layer such that said data pad is at least partially exposed; and

a data pad electrode electrically contacting said data pad via said contact hole.

30. A liquid crystal display according to claim 29, said data pad has a bent shape.

31. A liquid crystal display according to claim 29, wherein said data pad electrode contacts said gate insulation layer.